What is claimed is:

1. A method of manufacturing a semiconductor device in which a resistive conductive layer and a MOS transistor are provided on a same semiconductor layer, the method comprising:

forming a first insulating layer over the semiconductor layer in a formation region for the resistive conductive layer;

forming an elements isolation region in a formation region for the MOS transistor;

forming the resistive conductive layer on the first insulating layer in the formation region for the resistive conductive layer;

forming a protective layer so as to cover the resistive conductive layer in the formation region for the resistive conductive layer;

forming a second insulating layer on the semiconductor layer by exposing a surface of the semiconductor layer and thermally oxidizing the surface of the semiconductor layer in the formation region for the MOS transistor;

forming a gate conductive layer at least on the second insulating layer; and

forming a gate electrode and a gate insulating layer by patterning the gate conductive layer and the second insulating layer in the formation region for the MOS transistor.

2. A method of manufacturing a semiconductor device in which a resistive conductive layer and an MOS transistor are provided on a same semiconductor layer, the method comprising:

forming a first insulating layer over the semiconductor layer in a formation region for the resistive conductive layer;

forming an elements isolation region in a formation region for the MOS transistor;

forming the resistive conductive layer on the first insulating layer in the formation region for the resistive conductive layer;

forming a protective layer on the resistive conductive layer in the formation region for the resistive conductive layer;

forming a second insulating layer on the semiconductor layer by

exposing a surface of the semiconductor layer and thermally oxidizing the surface of the semiconductor layer in the formation region for the MOS transistor;

forming a third insulating layer on a side surface of the resistive conductive layer;

forming a gate conductive layer at least on the second insulating layer; and

forming a gate electrode and a gate insulating layer by patterning the gate conductive layer and the second insulating layer in the formation region for the MOS transistor.

3. The method of manufacturing a semiconductor device according to Claim 1 or Claim 2, wherein the gate conductive layer comprises a multi-layered structure including a polysilicon layer and a metal layer.

4. The method of manufacturing a semiconductor device according to any one of Claims 1 or 2, wherein the resistive conductive layer comprises a polysilicon layer.

5. The method of manufacturing a semiconductor device according to any one of Claims 1 or 2, wherein the first insulating layer and the elements isolation region are formed in a same step.

6. The method of manufacturing a semiconductor device according to Claim 5, wherein the first insulating layer and the elements isolation region are formed by oxidizing the surface of the semiconductor layer.

7. The method of manufacturing a semiconductor device according to any one of Claims 1 or 2 wherein the resistive conductive layer, and a high breakdown voltage transistor and a low breakdown voltage transistor of an insulated gate type are formed on the same semiconductor layer, the high breakdown voltage transistor including a proof voltage between a source and a drain of the high breakdown voltage transistor, which is different from that of the low breakdown voltage transistor, and the MOS transistor comprises the high breakdown voltage transistor.

8. The method of manufacturing a semiconductor device according to any one of Claims 1 or 2 wherein the second insulating layer is formed by exposing at least a region of the semiconductor layer on which to form the gate electrode

and then thermally oxidizing the surface thereof in the formation region for the MOS transistor.

9. The method of manufacturing a semiconductor device according to Claim 1, wherein the semiconductor layer comprises a layer including a silicon substrate on the surface thereof, wherein the first and the second insulating layers each comprise a silicon oxide layer, and wherein the protective layer comprises a silicon nitride layer or a silicon oxynitride layer.

10. The method of manufacturing a semiconductor device according to Claim 2, wherein the semiconductor layer comprises a layer including a silicon layer at least on the surface thereof, the first, the second and the third insulating layers each comprise a silicon oxide layer, and the protective layer comprises a silicon nitride layer or a silicon oxynitride layer.

11. The method of manufacturing a semiconductor device according to Claim 2, wherein the second insulating layer and the third insulating layer are formed in a same step.

12. The method of manufacturing a semiconductor device according to Claim 11, wherein each of the second insulating layer and the third insulating layer is formed by oxidizing the surface of the semiconductor layer and the side surface of the resistive conductive layer.

13. A semiconductor device, comprising:

a semiconductor layer;

an MOS transistor formed on the semiconductor layer; and

a resistive conductive layer formed on the semiconductor layer through an insulating layer, wherein;

the MOS transistor comprises a gate insulating layer and a gate electrode formed on the gate insulating layer.

14. The semiconductor device according to Claim 13, wherein the gate electrode comprises a multi-layered structure including a polysilicon layer and a metal layer.

15. The semiconductor device according to Claim 13 or Claim 14, wherein the resistive conductive layer comprises a polysilicon layer.

16. The semiconductor device according to any one of Claims 13 or 14, wherein the semiconductor layer comprises a layer including a silicon layer at least on the surface thereof, and the gate-insulating layer comprises a silicon oxide layer.

17. The semiconductor device according to any one of Claims 13 or 14, wherein a high breakdown voltage transistor and a low breakdown voltage transistor of insulated gate types are formed on the semiconductor layer, the high breakdown voltage transistor including a proof voltage between a source and a drain which is different from that of the low breakdown voltage transistor, and wherein the MOS transistor comprises the high breakdown voltage transistor.

18. The semiconductor device according to any one of Claims 13 or 14, further comprising a protective layer formed so as to cover the resistive conductive layer.

19. The semiconductor device according to any one of Claims 13 or 14, further comprising a protective layer formed on the resistive conductive layer.

20. The method of manufacturing a semiconductor device according to claim 1, wherein the step of forming the resistive conductive layer and the gate electrode are done separately.

21. The method of manufacturing a semiconductor device according to claim 2, wherein the step of forming the resistive conductive layer and the gate electrode are done separately.

22. The method of manufacturing a semiconductor device according to claim 2, wherein said step of forming the second insulating layer and the step of forming the third insulating layer are formed in a same step.

23. The method of manufacturing a semiconductor device according to claims 1 and 2, wherein the resistive conductive layer is doped with an impurity to create a predetermined resistance.

24. The semiconductor device according to claim 14, wherein said metal layer comprises a metal selected from the following group: tungsten and molybdenum.

25. The method of manufacturing a semiconductor device according to claim 8, wherein said exposing step and said oxidizing step are performed when said protective layer covers said resistive conductive layer.

26. The method of manufacturing a semiconductor device according to claim 3, wherein the resistive conductive layer comprises a polysilicon layer.

27. The method of manufacturing a semiconductor device according to claim 3, wherein the first insulating layer and the elements isolation region are formed in a same step.

28. The method of manufacturing a semiconductor device according to claim 4, wherein the first insulating layer and the elements isolation region are formed in a same step.

29. The semiconductor device according to claim 15, wherein the semiconductor layer comprises a layer including a silicon layer at least on the surface thereof, and the gate-insulating layer comprises a silicon oxide layer.

30. The semiconductor device according to claim 15, wherein a high breakdown voltage transistor and a low breakdown voltage transistor of insulated gate types are formed on the semiconductor layer, the high breakdown voltage transistor including a proof voltage between a source and a drain which is different from that of the low breakdown voltage transistor, and wherein the MOS transistor comprises the high breakdown voltage transistor.

31. The semiconductor device according to claim 16, wherein a high breakdown voltage transistor and a low breakdown voltage transistor of insulated gate types are formed on the semiconductor layer, the high breakdown voltage transistor including a proof voltage between a source and a drain which is different from that of the low breakdown voltage transistor, and wherein the MOS transistor comprises the high breakdown voltage transistor.

32. The method of manufacturing a semiconductor device according to claim 4, wherein the MOS transistor comprises a twin-well structure.

33. The method of manufacturing a semiconductor device according to claim 4, wherein the MOS transistor comprises a triple-well structure.